IN THE CLAIMS:

Claims 1-6 (Canceled).

Claim 7 (Currently Amended): A package substrate electrolytically plated with Au without using any plating lead line, comprising:

a base substrate formed with a plurality of through holes;

a first copper plated layer plated on predetermined portions of the base substrate, which serves as a plating lead line, and inner surfaces of the through holes;

a plated pattern layer formed on the first copper plated layer, the plated pattern layer including a second copper plated layer formed on portions of the first copper plated layer;

wire bonding pads formed on predetermined portions of the plated pattern layer at an upper surface of the base substrate where portions of ~~removed~~ the first copper plated layer have been removed ~~served as a plating lead line~~, the wire bonding pads including Au and not connected to a remnant of a plating lead line;

solder ball pads formed on predetermined portions of the plated pattern layer at a lower surface of the base substrate where portions of ~~removed~~ the first copper plated layer have been removed ~~served as a plating lead line~~, the solder ball pads including Au and not connected to a remnant of a plating lead line; and

a solder resist having a first portion contacting the upper surface of the base substrate and the plated pattern layer and a second portion contacting the lower surface of the base substrate and the solder ball pads.

Claim 8 (Original): The package substrate according to claim 7, wherein the wire bonding pads and the solder ball pads are Au layers plated in accordance with application of current to the first copper plated layer.

Claim 9 (Original): The package substrate according to claim 7, wherein the first copper plated layer serves as a plating lead line during the electrolytic Au plating processes for the solder ball pads and the wire bonding pads.

Claim 10 (Original): The package substrate according to claim 7, wherein each of the electrolytic Au plating process forms a plated layer having a thickness of 0.5 to 1.5μm.

Claim 11 (Original): The package substrate according to claim 7, wherein the first copper plated layer is an electroless copper plated layer.

Claim 12 (Previously Presented): The package substrate according to claim 7, wherein the base substrate is a copper clad laminate (CCL).

Claim 13 (Previously Presented): The package substrate according to claim 7, wherein the solder resist covers portions of the wire bonding pads or the solder ball pads, and exposes other portions of the wire bonding pads or the solder ball pads.

Claim 14 (Previously Presented): The package substrate according to claim 7, wherein the second copper plated layer fills the through holes.